From PERPLEXUS and DLL to ARUZ - a role of chance in scientific discovery

Andrzej NAPIERALSKI

1st of December 2016, Łódź

Technical University of Lodz

MORENO J.M., CASTILLO F., CABESTANY J., NAPIERALSKI A., MADRENAS J.: "An analog systolic VLSI architecture for implementing neural network models", IEEE MICRO, June 1994, pp. 51- 59

"VHDL macromodels for analogue-digital circuits" - "Makromodele VHDL dla układów analogowo-cyfrowych", ITE, Warsaw, Research Project nr 8 T11 B 001 11. (Project leader A. Napieralski – PhD grant - Robert Baraniecki). 01.07.1996-30.06.1998.

5thPhD Thesis defense 17.07.1998 in Institute of Electron Technology - Warsaw. Thesis received distinction and the Prize of First Minister of Poland.

„Application of High Level VHDL-AMS Language to Computer Modelling, Design and Realisation of Integrated Microsystems” - "Zastosowanie języka wysokiego poziomu VHDL-A do celów komputerowego modelowania, projektowania i realizacji mikrosystemów scalonych". Lodz University of Technology 1997. Research Project Nr. 8 T11F 010 12, (Project leader A. Napieralski). 1997-2000

NATO Grant:

"Advanced Computer tools For Thermal Analysis of Power Cables". *No. 960050. Project with ONTARIO HYDRO, Toronto, Ontario, Canada. 01.05.1996 - 30.04.1998.*

„Systolic neural processor with build in learning algorithm. Design and realisation in VLSI technology”. „Systoliczny procesor neuronowy z wbudowanym algorytmem uczenia – realizacja w technologii VLSI. Praktyczne zastosowanie do problemu wykrywania wycieków oleju z kabli wysokiego napięcia”. Projekt badawczy 8 T11B 029 15, (Project leader A. Napieralski - PhD grant - Cezary Bolek). 1998-2000

14thPhD. Cezary BOLEK: “VLSI Systolic Neural Processor with Built-in Learning Capability. Field Application for Oil Leakage Detection of High Voltage Cables”. “Systoliczny procesor neuronowy wykonany w technologii VLSI z wbudowanym algorytmem uczenia. Zastosowanie do detekcji wycieków oleju w kablach wysokonapięciowych”. Thesis defense 13.06.2001.

„High Level Algorithm of partition of the dynamically reconfigurable integrated circuits with the possibility of multicontecst reconfiguration” - „Wysokopoziomowy algorytm partycjonowania dedykowany układom dynamicznie rekonfigurowalnym z możliwością rekonfiguracji wielokontekstowej”. Projekt badawczy 8 T11B 004 24, (Project leader A. Napieralski - PhD grant - Rafał Kiełbik). 2003.

18thPhD. Rafał KIEŁBIK: „Efficient methods of resource management in reprogrammable systems” - (Efektywne metody wykorzystywania zasobów systemów reprogramowalnych). Defense in Poland 10.06.2005. Defense in UPC in Barcelona 25.05.2006. Co-supervisor prof. Manuel Moreno Arostegui. *Thesis received distinction*

"Pervasive computing framework for modeling complex virtually-unbounded systems – PERPLEXUS" *- "Rozproszona Platforma Obliczeniowa do Modelowania Złożonych Systemów Pozornie Nieograniczonych"* ***Proposal/Contract No.: 34632. Date of preparation of Annex1: 21.03.2006, Operative commencement date of contract: 01.09.2006.***

Partners:

1. ***Haute Ecole d'Ingénierie et de Gestion du Canton de Vaud - HEIG-VD, Switzerland.***
2. ***Universitat Politecnica de Catalunya – UPC, Spain***
3. ***Université Joseph Fournier Grenoble 1 - UJF, France***
4. ***Université de Lausanne – UNIL, Switzerland***
5. ***Politechnika Łódzka – TUL – Poland***
6. ***Centre National de la Recherche Scientifique – CNRS, France***
7. ***WANY Robotics – WANY, France***
8. ***SCIPROM – Scientific project management – SCIPROM, Switzerland***

Abstract: We will develop a scalable hardware platform made of custom reconfigurable devices endowed with bio−inspired capabilities that will enable the simulation of large−scale complex systems and the study of emergent complex behaviors in a virtually unbounded wireless network of computing modules. At the heart of these **ubiquitous computing modules** (**ubidules**), we will use a custom reconfigurable electronic device capable of implementing bio−inspired mechanisms such as growth, learning, and evolution. This reconfigurable circuit will be associated to rich sensory elements and wireless communication capabilities.

The Authors

Eduardo Sanchez, Andres Perez-Uribe, Andres Upegui, Yann Thoma (HEIG-VD, Switzerland), Juan Manuel Moreno (UPC, Spain), Alessandro Villa (UJF, France), Henri Volken (UNIL, Switzerland), Andrzej Napieralski (TUL, Poland), Gilles Sassatelli (CNRS, France), Erwan Lavarec (Wany Robotics,France)

of paper

'PERPLEXUS: Pervasive Computing Framework for Modeling Complex Virtually-Unbound Systems'

have won the prize in the

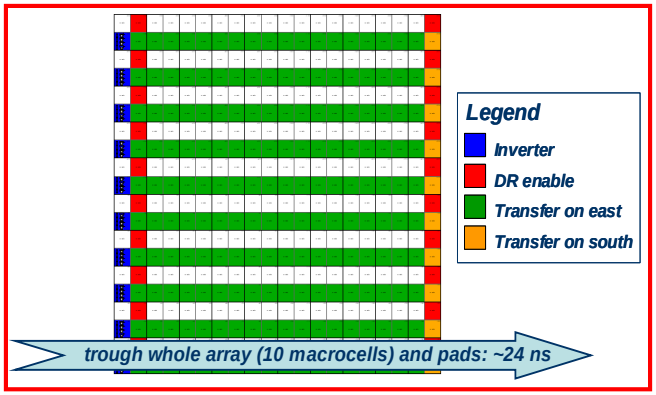
Future and Emerging Technologies category

at the

AHS 2007 Conference

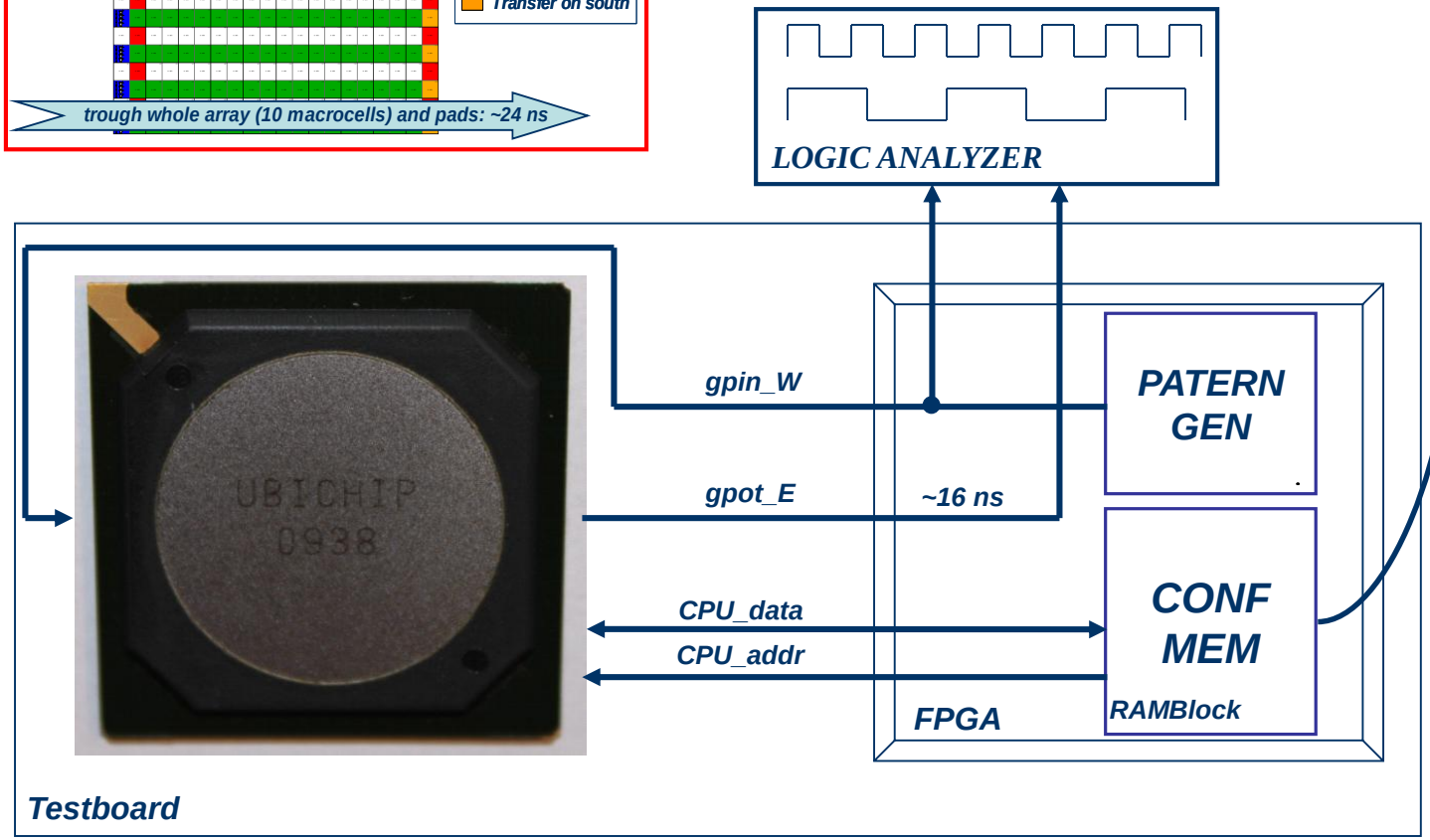
held at The University of Edinburgh
5th - 8th August 2007

*Second NASA/ESA Conference on **A**daptive **H**ardware and **S**ystems*



Tests controlled by PC

NATIVE test



Dedicated parallel machines - a breakthrough in computation

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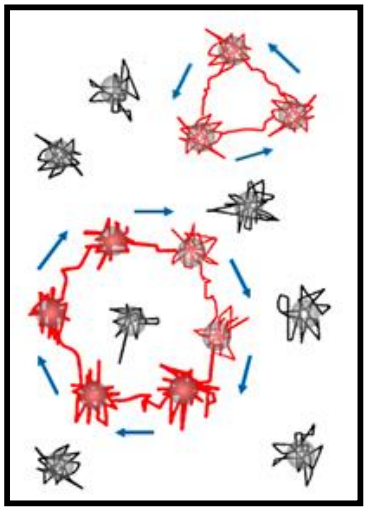
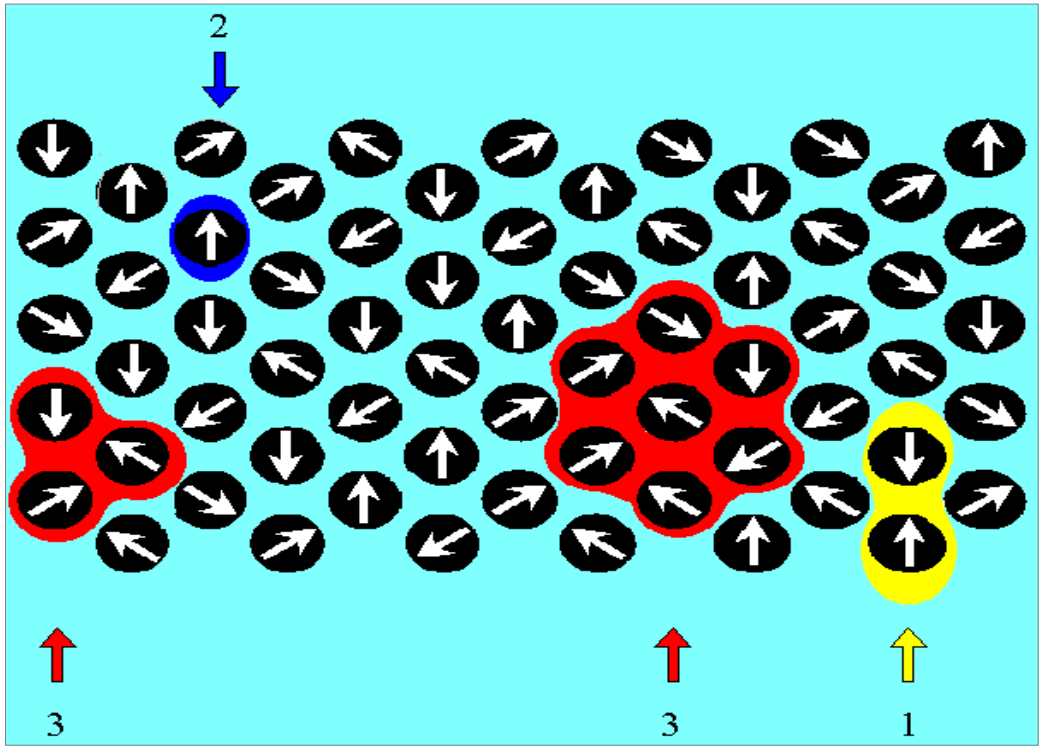
Prof. T. Pakuła, PŁ



Inspiration: Dynamic Lattice Liquid (DLL) Algorithm

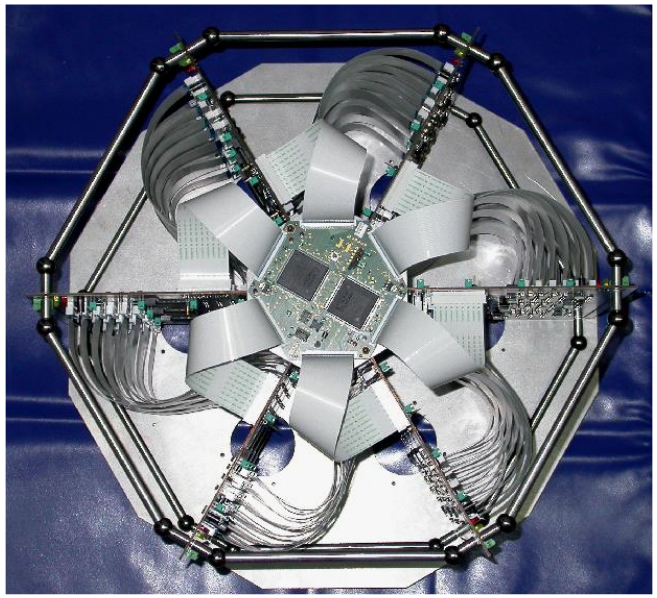


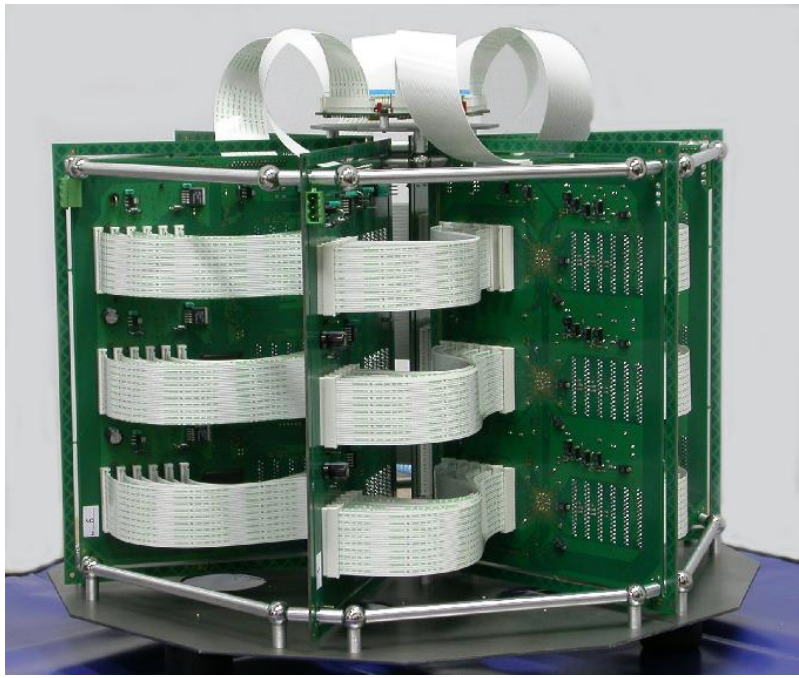
2002

First Approach

2006 – 2008: Grant of Polish Ministry of Science and Higher Education: **„Implementation of Dynamic Lattice Liquid Algorithm by Means of Dedicated Microprogrammable Computational Cell”**, 299 750 PLN

Result: (**μDLL**):
6x6x6 = **216 nodes** (18 FPGAs)





Nr 3361/B/T02/2009/36. 25.06.2009–24.06.2012

„Module of Dedicated Computational Cluster for Simulations Based on Dynamic Lattice Liquid Algorithm”, - *„Moduł dedykowanego klastra obliczeniowego realizującego algorytm Dynamicznej Cieczy Sieciowej”.* **(dr Rafał Kiełbik)**

2009 – 2012: Grant of Polish Ministry of Science and Higher Education:
„**Module of Dedicated Computational Cluster for Simulations Based on Dynamic Lattice Liquid Algorithm**”, 497 900 PLN

Scalable Prototype

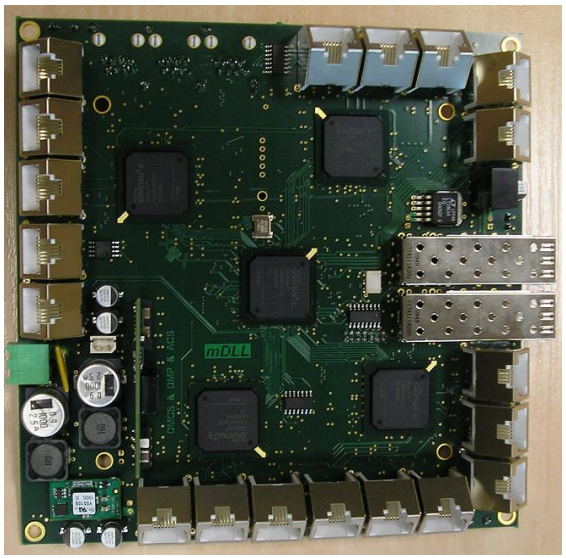
Result (**mDLL**):

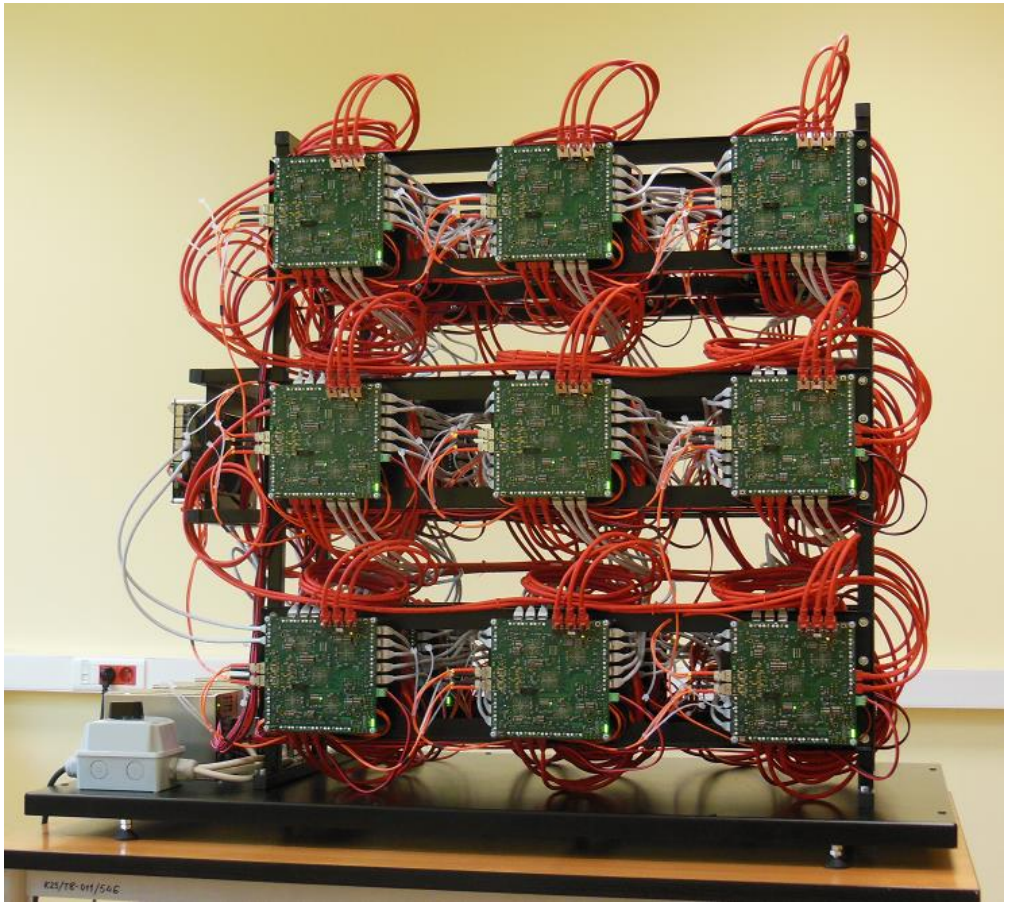
28 modules, 5 FPGAs in each module

(4 for simulations, 1 for controlling),

~64 nodes (in each FPGA).

In total: **~1 728 nodes** (140 FPGAs)





6036/B/T02/2010/39. 30.09.2010-29.03.2012

"Tools developement for design of the dynamically reconfigurable digital circuits" - *"Opracowanie narzędzi wspomagających projektowanie cyfrowych układów dynamicznie rekonfigurowalnych"* - Project leader A. Napieralski - PhD grant Piotr Amrozik.

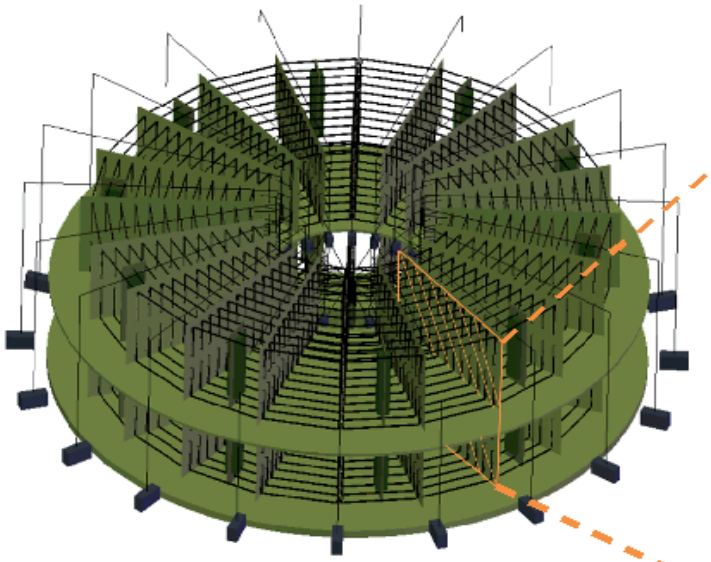
Nr 2011/01/N/ST7/05242 2011-2013

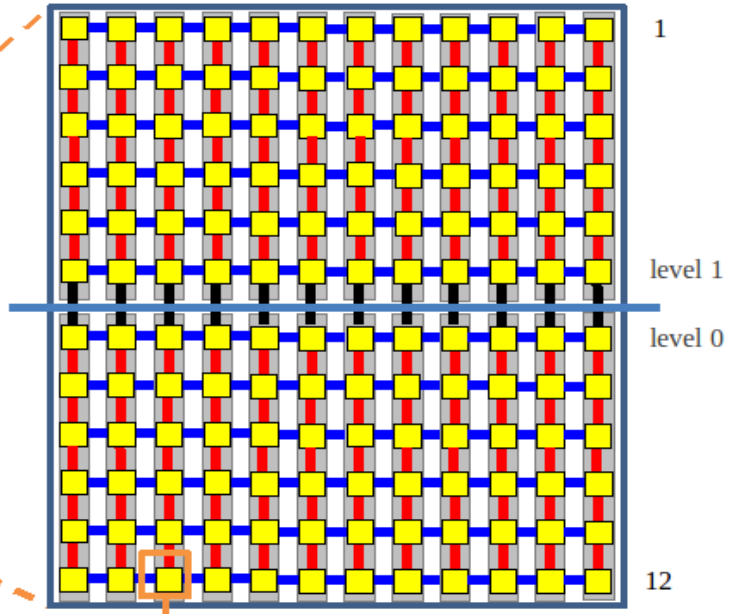
„Microarchitecture of computational elements for general purpose reconfigurable processor" - *Mikroarchitektura elementów obliczeniowych dla rekonfigurowalnego procesora ogólnego przeznaczenia* (P. Amrozik)

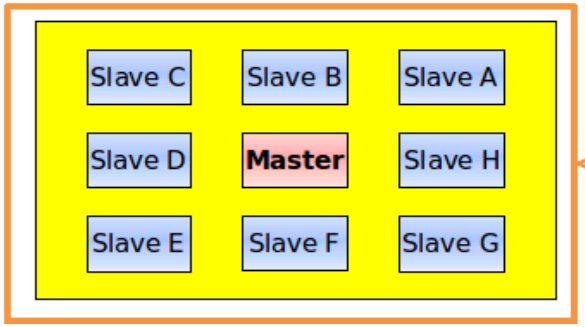
46th PhD. Piotr AMROZIK: "Modular Dynamically Reconfigurable Circuits Design Methodology". Defended 02.07.2012.

NCN/Preludium 6 2016-2019

Tytuł: Metody programowania rozproszonych systemów rekonfigurowalnych (J. Kupis)







144 x DBoard

In total:

- 2 880 PCB boards
- 25 920 FPGAs
- **~1 500 000 nodes**

Dedicated parallel machines - a breakthrough in computation

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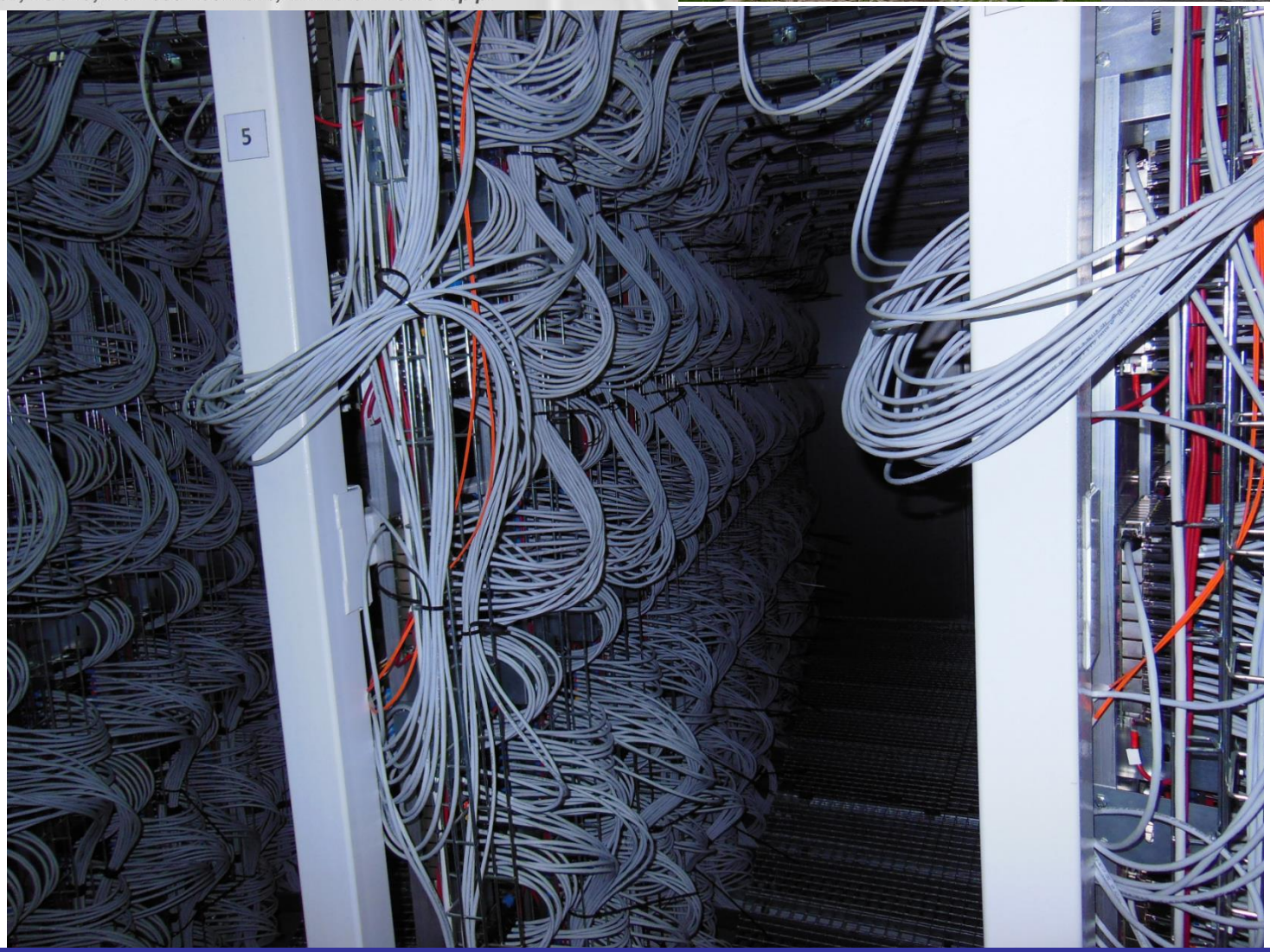

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Patents

1. *JUNG J., POLANOWSKI P., KIEŁBIK R., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A.: „Panel z układami elektronicznymi i zestaw paneli”. Wniosek patentowy zarejestrowany w dniu 30.09.2013r nr P.405479.*
2. *JUNG J., POLANOWSKI P., KIEŁBIK R., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A.: ”Maszyna równoległa z komórkami operacyjnymi umieszczonymi w węzłach sieci powierzchniowo centrowanej”. Wniosek patentowy zarejestrowany w dniu 30.09.2013r nr P.40548*
3. *JUNG J., POLANOWSKI P., KIEŁBIK R., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A.: „Maszyna równoległa ze zredukowaną liczbą połączeń pomiędzy układami logicznymi”. Wniosek patentowy zarejestrowany w dniu 30.09.2013r nr P.405481.*

4. *JUNG J., POLANOWSKI P., KIEŁBIK R., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A.: „System modułów elektronicznych o redundantnej konfiguracji”. Wniosek patentowy zarejestrowany w dniu 30.09.2013r nr P.405482.*
5. *KIEŁBIK R., AMROZIK P., NAPIERALSKI A., JABŁOŃSKI G., ZAJĄC P., ZARZYCKI I.: "Układ FPGA i sposób sterowania dostępem do pamięci zewnętrznej w układzie FPGA". Data zgłoszenia wniosku: 01.02.2014 r., nr wniosku: P.407040.*
6. *KIEŁBIK R., AMROZIK P., NAPIERALSKI A., JABŁOŃSKI G., ZAJĄC P., ZARZYCKI I.: "Układ FPGA oraz sposób aktywowania i dezaktywowania partycji", Data zgłoszenia: 01.02.2014 r. nr wniosku: P.407041.*

7. *JUNG J., POLANOWSKI P., KIEŁBIK R., HAŁAGAN K., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A, PAKUŁA T.: „A panel with electronic circuits and a set of panels", Data zgłoszenia do Europejskiego Urzędu Patentowego: 10.04.2015 r., nr wniosku: EP15163077.9*
8. *JUNG J., POLANOWSKI P., KIEŁBIK R., HAŁAGAN K., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A, PAKUŁA T.: „A parallel machine having operational cells located at nodes of a face centered lattice", Data zgłoszenia do Europejskiego Urzędu Patentowego: 10.04.2015 r., nr wniosku: EP15163078.7*
9. *JUNG J., POLANOWSKI P., KIEŁBIK R., HAŁAGAN K., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A., PAKUŁA T.: „A parallel machine with reduced number of connections between logical circuits", Data zgłoszenia do Europejskiego Urzędu Patentowego: 10.04.2015 r., nr wniosku: EP15163079.5*
10. *JUNG J., POLANOWSKI P., KIEŁBIK R., HAŁAGAN K., ZATORSKI W., ULAŃSKI J., NAPIERALSKI A, PAKUŁA T.: „System of electronic modules having a redundant configuration", Data zgłoszenia do Europejskiego Urzędu Patentowego: 10.04.2015 r., nr wniosku: EP15163080.3*

Thank You!

PERPLEXUS: Pervasive Computing Framework for Modeling Complex Virtually-Unbounded Systems

Eduardo Sanchez, Andres Perez-Uribe, Andres Upegui, Yann Thoma
HEIG-VD, Switzerland
(eduardo.sanchez, andres.perez-uribe, andres.upegui, yann.thoma)@heig-vd.ch

Juan Manuel Moreno
UPC, Spain
moreno@eel.upc.edu

Alessandro Villa
UJF, France
avilla@neuroheuristic.org

Henri Volken
UNIL, Switzerland
henri.volken@unil.ch

Andrzej Napieralski
TUL, Poland
napier@dmcs.p.lodz.pl

Gilles Sassatelli
CNRS, France
sassatelli@lirmm.fr

Erwan Lavarec
Wany Robotics, France
lavarec@wanyrobotics.com

Abstract: We will develop a scalable hardware platform made of custom reconfigurable devices endowed with bio−inspired capabilities that will enable the simulation of large−scale complex systems and the study of emergent complex behaviors in a virtually unbounded wireless network of computing modules. At the heart of these **ubiquitous computing modules** (**ubidules**), we will use a custom reconfigurable electronic device capable of implementing bio−inspired mechanisms such as growth, learning, and evolution. This reconfigurable circuit will be associated to rich sensory elements and wireless communication capabilities.

Such an infrastructure will provide several advantages compared to classical software simulations: speed−up, an inherent real−time interaction with the environment, self−organization capabilities, simulation in the presence of uncertainty, and distributed multi−scale simulations.

The strong interaction between our hardware infrastructure and the real environment circumvent the need to simulate the environment and ease the occurrence of unexpected emergent phenomena. The observation of such emergent phenomena will be now facilitated by the shorter simulation time, brought by the hardware speed−up. One of the major difficulties of a complex system simulation is to define the structural organization of the modules composing the model. The self−organization and bio−inspired capabilities of our platform will bring an innovative solution to this problem: an evolving and hierarchical structure. The function of each ubidule can be dynamically and autonomously determined by the simulation itself: it can be an independent agent or a part of a largest entity. We have identified four domains where our modeling infrastructure will prove its usefulness as a powerful and innovative simulation tool: biologically−plausible developing neural networks modeling, culture dissemination modeling, gene−regulatory networks modeling, and cooperative collective robotics modeling.

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